Intel® IXD1110 Demo Board

Development Kit Manual

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11	Added second bullet under Section 2.0, “Quick Start”.
13	Modified Figure 3, “Intel® IXF1110 CPU Daughter Card”.
16	Added Section 5.3, “Changing the IP Address of the CPU Daughter Card (Optional)”.
18	Added note under Section 6.2, “JTAG Test Signals”.
18	Modified pin 8 description in Table 3, “JTAG Test Signals (JP1)”.
19	Modified Table 4, “IXF1110 LED Behavior”.

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14	Modified bulleted list under Section 4.2, “IXF1110 Register Modifications on Startup”.

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1.0 Introduction

This document describes all the necessary requirements, settings, and procedures for evaluating the Intel® IXF1110 10-Port 1000 Mbps Ethernet Media Access Controller (MAC) using the Intel® IXD1110 demo board. For immediate operation, refer to Section 2.0, "Quick Start" on page 11. For optional configurations, see Section 6.0, "Optional Configurations" on page 18.

The IXD1110 demo board kit includes a CPU daughter card that attaches to the underside of the board. Through the CPU daughter card, the Intel® IXF1010/IXF1110 10-Port 100/1000 Ethernet MAC Demonstration Software (included on the CD) provides access to all IXF1110 registers and RMON statistics.

Additional sections include information about LEDs, test points, board schematics, and a bill of materials.

Note: For comprehensive information in evaluating the IXF1110 using the IXD1110 demo board, use the IXF1110 Demonstration Software Help File and the IXF1110 Datasheet (document number 250210) in conjunction with this document.

1.1 About This Kit

The IXD1110 demo board kit includes the following:

- IXD1110 demo board with CPU daughter card
- IXF1110 Demonstration Software CD (includes a software help file)
- SPI4-2 loopback connector
- IXD1110 Demo Board Development Kit Manual

1.2 Additional Equipment Required

The following additional equipment is required for board setup:

- Packet Generator with 1000BASE-SX capabilities
- 3.3 V DC power supply with 6A current capability
- 2.5 V DC power supply with 6A current capability
- 1.8 V DC power supply with 6A current capability
- One to ten fiber cables (for data transmission)
- Two CAT5-UTP cables (for IXF1110 software)
- DB-9–to–RJ-45 converter [optional] (for IXF1110 software)
- PC (for IXF1110 software) (see Section 5.1, "PC Requirements" on page 15)
- GBIC SFP modules [up to 10] (Agilent* HFBR-5710L)

1.3 About The IXD1110 Demo Board

The IXD1110 demo board provides a working platform for the evaluation of the IXF1110 in 1000 Mbps fiber optic applications. All ten network ports provide a 1000BASE-SX connection through the GBIC Small Form Factor Pluggable (SFP) modules (not included).

The IXD1110 demo board contains one IXF1110 device, one SPI4-2 interface connector, ten GBIC SFP connectors, and one plug-in CPU daughter card. The SPI4-2 interface connector allows for loopback connection.

Note: In loopback mode, the board cannot be tested or used with other devices or equipment.

Connection can be made to an alternate SPI4-2 device or to another IXD1010 or IXD1110 demo board utilizing a SPI4-2 connector board. In these modes, the SPI4-2 interface can be tested for lengths greater than that in loopback mode.

The attached CPU daughter card uses the IXF1110 CPU interface to access all registers and RMON statistics through the supplied IXF1110 software.

1.3.1 Features

The following is a list of IXD1110 demo board features and evaluation capabilities:

- Ten IEEE 802.3 compliant 1000BASE-SX MAC ports
- SPI4-2 interface
  - — Capable of data transfers up to 12.8 Gbps
  - — Supports SPI4-2 loopback mode (default)
  - — Can be connected to another SPI4-2 device (optional)
    For example, a SPI4-2 enabled daughter card (FPGAs, bridges, etc.)
- SerDes interface with GBIC SFP modules not included
- Motorola* MCP860 32-bit CPU
  - — Mounted on the daughter card, which is attached to the bottom side of the demo board (see Figure 2)
- Access to all supported registers for full evaluation
- Access to all RMON statistics registers
- Broadcast, multicast, and unicast address filtering capability
- Independent port enable/disable
- Programmable option to filter packets with errors
- Compliance with IEEE 802.3x flow control standard

1.3.2 Component Location and Description

Figure 1 illustrates the top view of the IXD1110 demo board.

Figure 1. Intel® IXD1110 Demo Board (Top View)

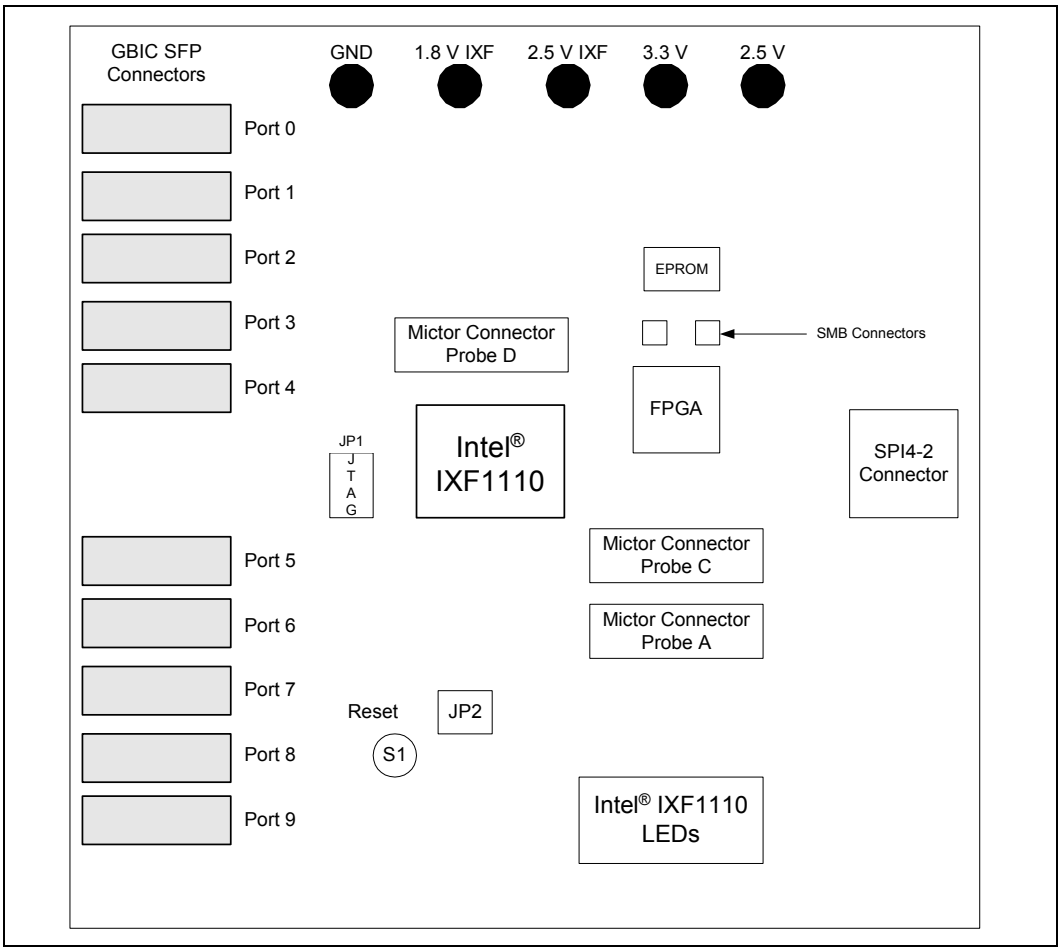


Table 1 provides a list of the various principal components found on the IXD1110 demo board.

Table 1. Intel® IXD1110 Demo Board Principal Components

Component	Description
IXF1110	10-port Gigabit MAC that supports IEEE 802.3 1000 Mbps applications. Refer to the IXF1110 Datasheet for additional information.
IXF1110 LEDs	The IXF1110 uses a serial interface consisting of three signals to provide LED data to an external driver. This interface provides the data for 30 separate direct drive LEDs and allows three LEDs per MAC port. Refer to Section 7.0, “LEDs” on page 19.
JP1	This jumper provides access to the JTAG test signals. Refer to Section 6.2, “JTAG Test Signals” on page 18.
JP2	This reset jumper is required for proper board operation. Refer to Section 6.1, “Reset Jumper JP2” on page 18 for more information.
1. For evaluation of the signals provided by the Mictor connector, use the corresponding logic analyzer probe.	

Table 1. Intel® IXD1110 Demo Board Principal Components (Continued)

Component	Description
S1	Reset Switch: This switch resets the entire board when pressed.
SPI4-2 Interface Connector	Allows a loopback connection when the loopback module is installed. This connector can also interface with alternate SPI4-2 connections.
Mictor Connectors A, C, and D[1]	Provide access to selected IXF1110 signals. Refer to Section 8.4, "Mictor Connectors" on page 21 for more information.
GBIC Connectors	These connectors allow for SFP modules (Agilent* HFBR-5710L).
FPGA	Converts the IXF11110 asynchronous CPU signals into a synchronous format. Refer to Section 4.1, "CPU FPGA" on page 14 for more information.
EPROM	EPROM is used to program the FPGA.
1. For evaluation of the signals provided by the Mictor connector, use the corresponding logic analyzer probe.	

2.0 Quick Start

The quick-start procedure allows for IXF1110 1000 Mbps SerDes data transfer evaluation in the following interfaces:

- IXF1110 SPI4-2 loopback data transfer
- I^2C signals
- CPU interface

2.1 Setup

The following quick-start procedure uses the IXIA* 1600T packet generator to evaluate the IXD1110 demo board. All ports on the IXF1110 are set to a default setting of 1000 Mbps full-duplex (see Figure 2, “Typical Test Setup” on page 12).

1. Set reset jumper JP2 to the HRESET position.
2. Jumper pins 6 and 8 of JP1.
3. Install optic modules on all ten ports.
4. Connect the IXF1110 optic modules to the external ports on the IXIA* 1600T LM1000SX cards.
5. Verify that the CPU daughter card is installed on the bottom of the board.
6. Verify that the SPI4-2 loopback module is connected to the SPI4-2 connector.
7. Connect the 1.8 V DC power supply to BN1 (“1.8 V IXF”).
8. Connect the 2.5 V DC power supply to BN4 (“2.5 V IXF”) and BN5 (“2.5 V”).
9. Connect the 3.3 V DC power supply to BN6 (“3.3 V”).
10. Connect all power supply return lines to ground BN3 (“GND”).
11. With the board properly configured, proceed in the following order:
    a. Apply +1.8 V DC power
    b. Apply +2.5 V DC power
    c. Apply+3.3 V, DC power
    d. Press reset switch S1
12. Once the CPU Daughter Card has completed autoboot, the board is ready for evaluation of standard packets (64 - 1518 bytes) at 1000 Mbps full-duplex on all ports.
13. To access registers and RMON statistics, install the IXF1110 software. Instructions are provided in Section 5.2, “Installing the IXF1110 Software” on page 16. This allows the user to change the default settings of the IXF1110 and configure the device for other modes of operation.
14. Proceed with evaluation as desired.

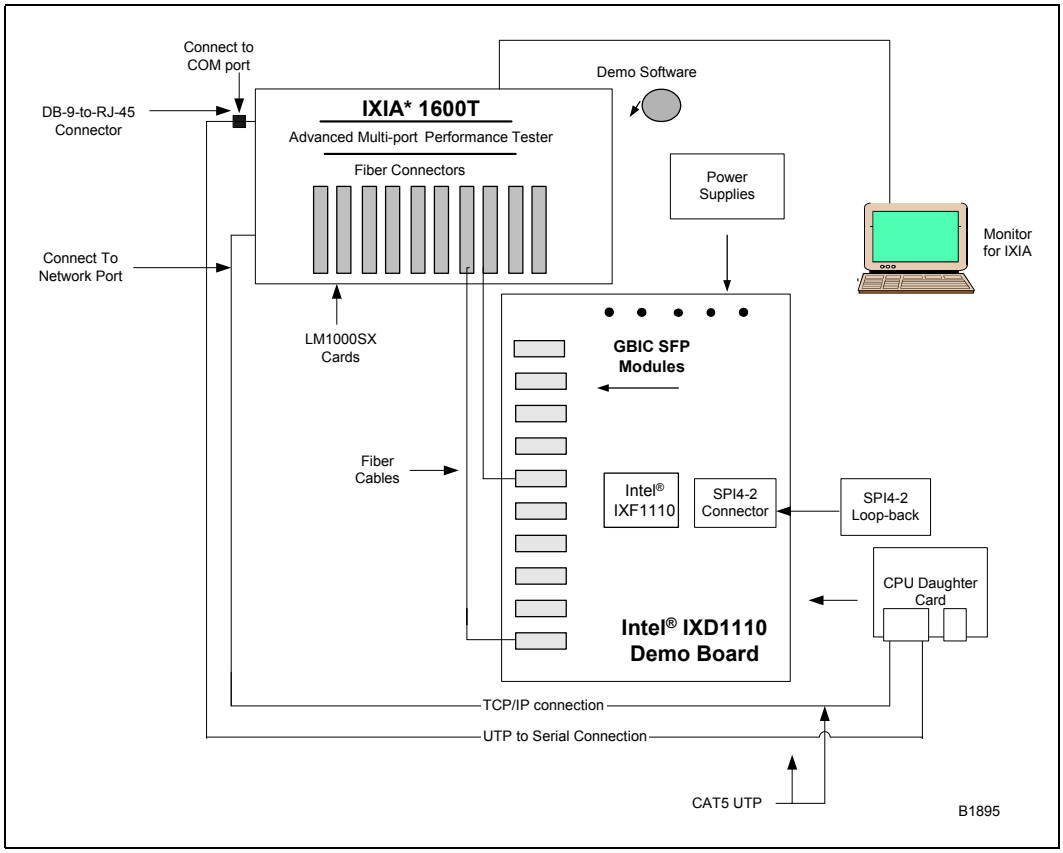
Note: The IXF1110 software modifies some of the IXF1110 registers on power-up. For a complete list of registers modified, please refer to Section 4.2, “IXF1110 Register Modifications on Startup” on page 14.

3.0 Typical Test Setup

Figure 2 shows a typical test setup for standard operation of the IXF1110 (see Section 2.0, "Quick Start" on page 11 for step-by-step details). The IXD1110 demo board can be connected to an IXIA* 1600T packet generator with LM1000SX cards for evaluation of the board. Each port can be connected to the IXIA* box with fiber cables. For IXF1110 software use, connect CAT5-UTP cables to the ports shown on the CPU daughter card. One of the cables connects to the COM port on the IXIA* box by using a DB-9–to–RJ-45 connector. The other cable connects to the network port on the IXIA* box. Refer to Figure 2 and Section 5.2, "Installing the IXF1110 Software" on page 16 for proper installation.

Note: The IXF1110 evaluation software can be run from the IXIA or an added PC connected to the CPU daughter card.

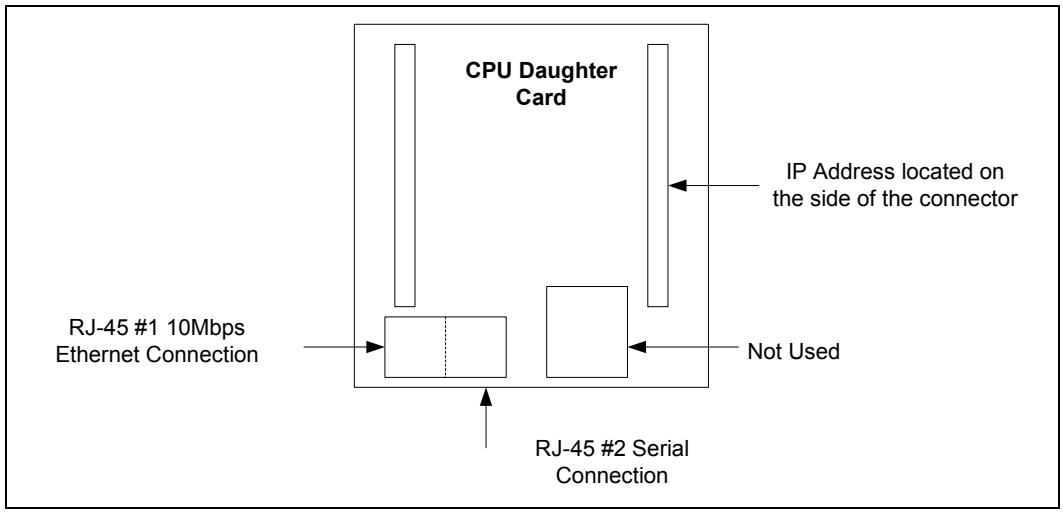
Figure 2. Typical Test Setup



4.0 CPU Daughter Card

The IXD1110 demo board uses the Embedded Planet* RPX Classic LF (CLLF_BW31), a single-board computer that uses the Motorola* MPC860 CPU. This card attaches to the underside of the board and is used to interface with the IXF1110 CPU interface. Figure 3 provides a top-level view of the CPU daughter card.

Figure 3. Intel® IXF1110 CPU Daughter Card


CPU Daughter Card
IP Address located on the side of the connector
RJ-45 #1 10Mbps Ethernet Connection
Not Used
RJ-45 #2 Serial Connection

The IXF1110 software requires the proper connections to the daughter card as follows:

Note: For full operation of the IXF1110 software, RJ-45 #1 and #2 (see Figure 3) must be connected to a PC.

- RJ-45 #1 (10 Mbps Ethernet): Requires the following connection (this connection gives access to the GUI):
  - — CAT5-UTP cable (connected to the CPU daughter card)
  - — Network port on a PC (connected to the CAT5-UTP cable), installed with IXF1110 software
- RJ-45 #2 (Serial): Requires a connection that gives access to the HyperTerminal interface of the IXF1010 software (refer to Section 5.2, “Installing the IXF1110 Software” on page 16 for complete setup information).
- Table 2 provides the DB-9–to–RJ-45 connector pinout for connection to a PC COM port. Only three pins are used for the DB-9–to–RJ-45 connector.

Table 2. Pinout for DB-9–to–RJ-45 Connector

RJ-45 Pin Number	DB-9 Pin Number
4	5
5	3
6	2

For more information on the HyperTerminal and GUI interfaces, please refer to the IXF1110 Software Help File.

4.1 CPU FPGA

The IXD1110 demo board has a Field Programmable Gate Array (FPGA) that allows the Motorola* CPU, which requires a synchronous interface, to interoperate with the asynchronous IXF1110 CPU interface.

For additional information regarding the IXF1110 CPU interface, refer to the IXF1110 Datasheet.

4.2 IXF1110 Register Modifications on Startup

The Motorola* CPU automatically modifies some of the IXF1110 registers on startup to put the board in a 1000 Mbps evaluation mode. The following registers are modified from default settings on startup:

- TX FIFO Highwater Mark Ports 0-9 are set to 0x00000BB8
- RX FIFO Errored Frame Drop Enable is set to 0x000003FF
- MAC Transfer Threshold Ports 0-9 are set to 0x000003E8
- Diverse Config Ports 0-9 are set to 0x0000112D
- LED Control is set to 0x00000003

For additional information on these registers, please refer to the IXF1110 Datasheet.

5.0 IXF1110 Software

The IXF1110 software allows access to the following register blocks through the Graphical User Interface (GUI) or the Serial Monitor (HyperTerminal) interface:

- MAC Control
- MAC RX Statistics
- MAC TX Statistics
- Global Status and Configuration
- RX Block
- TX Block
- SPI4-2 Block
- SerDes Block
- GBIC Block

For additional information on all of the registers, please refer to the IXF1110 Datasheet or On-Line Help.

Note: For help on using IXF1110 software, refer to the On-Line Help included in the software provided with the IXD1110 demo board.

5.1 PC Requirements

The following is a list of the minimum PC requirements for installation of the IXF1110 software:

- Intel® Pentium® II 400 MHz or equivalent
- 128 MB RAM
- 16 MB Video Card
- Serial port
- Microsoft* Windows 98, 2000 operating system

Note: Microsoft* Windows 95, ME, NT, and XP have not been tested.

- Microsoft* Windows HyperTerminal
- 1024 x 768 minimum viewing resolution

5.2 Installing the IXF1110 Software

For proper installation of the IXF1110 software, follow these steps:

1. Verify that the CAT5-UTP cable is connected between the PC and the IXF1110 CPU daughter card. This allows access to the GUI interface. Refer to Section 4.0, "CPU Daughter Card" on page 13 for detailed installation instructions.
2. **(Optional)** The following connection is required to access the HyperTerminal interface:
   - CAT5-UTP cable (connected to a CPU daughter card)
   - DB-9–to–RJ-45 connector (connected to a CAT5-UTP cable)
   - DB-9–to–RJ-45 connector (connected to a COM port on a PC installed with IXF1110 software)

     For more information, refer to Section 4.0, "CPU Daughter Card" on page 13 for detailed instructions.
3. Insert the CD into the PC.
4. If your system supports Autorun, follow the on-screen instructions.
5. If your system does not support Autorun, select **Run..**. from the **Start** menu. The *Run* dialog opens.
6. Select *setup.exe* from the CD in the **Open:** window (click **Browse...** to find *setup.exe* if not already in the window).
7. Click **OK**.
8. Follow the on-screen instructions.
9. Locate the IXD1110 demo board IP address that is located on the CPU daughter card. The IP address is required each time the GUI is opened.
10. Start the IXF1110 software GUI by double clicking the desktop icon.

Note: The IXF1110 software includes online documentation that describes how to run the GUI and HyperTerminal interfaces. Refer to the quick-start section of the IXF1110 Demonstration Software Help File for additional instructions on use of these interfaces.

5.3 Changing the IP Address of the CPU Daughter Card (Optional)

The CPU daughter card comes with a default IP address, which is listed on a sticker attached to the daughter card. The GUI uses this IP address to locate the IXD1110 demo board. The IP address may need to be changed depending on the PC or network to which the board is attached. Use the following procedure to permanently change the IP Address of the CPU daughter card:

1. Ensure the IXD1110 demo board has been set up correctly (see Section 2.0, "Quick Start" on page 11).
2. Open the HyperTerminal on the PC to which the CPU daughter card serial port is attached, and configure the relevant COM port with the following settings:

- Speed: 9600 Baud
- Databits: 8

- Parity: None
- Stops bits: 1
- Flow Control: None

3. Press the reset button switch SW1. The following message appears on the HyperTerminal:

   MPC8xx PlanetCore Boot Loader v2.00
   Copyright 2001 Embedded Planet. All rights reserved.
   DRAM available size = 16 MB
   wvCV
   DRAM OK
   Autoboot in 2 seconds.
   ESC to abort, SPACE or ENTER to go.

4. Press the ESC key to stop the Autoboot. The following message appears on the HyperTerminal:

   Autoboot aborted.
   >

5. Type the following at the > prompt:

   > set ip 10.254.21.34 *(Changes the IP address to the value entered)*

   > store *(Permanently changes the IP address)*

   > reset *(Restarts the IXD1110 demo board)*

Once the Autoboot is complete, the GUI can access the IXD1110 demo board using the newly programmed IP address.

6.0 Optional Configurations

6.1 Reset Jumper JP2

6.1.1 Standard Operation

The Reset Jumper JP2 is required for standard operation of the IXD1110 demo board. Use the HRESET position for standard operation.

The POR position is not recommended for standard operation of the IXD1110 demo board. This configuration only affects the CPU operation, and does not affect IXF1110 operation. The only difference between HRESET and POR is that POR also resets the CPU PLLs and state machines. This difference is seen when reset is asserted by pressing switch S1. For more information on the POR position of JP2, refer to Table 12 (MPC860 Reset Responses) of the Motorola* MPC860 CPU Datasheet.

6.2 JTAG Test Signals

The boundary scan test port for the IXF1110 is accessed using JP1 for board-level testing. Table 3 describes JTAG test signals.

Note: For normal IXD1110 demo board operation, connect TRST_N pin 8 on JP1 to ground by jumpering pins 6 and 8 of JP1.

Table 3. JTAG Test Signals (JP1)

Jumper	Pin Number	Symbol	IXF1110 Ball Designator	Description
JP1	1	TDI	AC18	Test Data Input
	3	TDO	Y24	Test Data Output
	5	TMS	T16	Test Mode Select
	7	TCLK	AA29	Test Clock
	8	TRST	N18	Test Reset (jumper pins 6 and 8)
	2,4,6	GND	–	Connect to system ground

7.0 LEDs

Table 4 describes the behavior of the Link LED - Amber, Link LED - Green, and Activity LED for the IXF1110.

Table 4. IXF1110 LED Behavior

Type	Status	Description
RxLED	Off	Synchronization has occurred but no packets are being received and the Link LED Enable Register (Addr: 0x502) is not set.
	Amber On	RX Synchronization has not occurred or no optical signal exists.
	Amber Blinking	Port has remote fault and the LED Fault Disable Register (Addr: 0x50B) is not set. Based on remote fault bit setting received in Rx_Config word.
	Green On	RX Synchronization has occurred and the Link LED Enable Register (Addr: 0x502) bit is set.
	Green Blinking	RX Synchronization has occurred and port is receiving data.
TxLED	Off	Port is not transmitting data or the Link LED Enable Register (Addr: 0x502)" is not set.
	Green Blinking	Port is transmitting data and the Link LED Enable Register (Addr: 0x502)" bit is set.

NOTES:
1. The LED behavior table assumes the port is enabled in the Port Enable Register (Addr: 0x500) and the LEDs are enabled in the LED Control Register (Addr: 0x509). If a port is not enabled, all the LEDs for that port will be off. If the LEDs are not enabled, all of the LEDs will be off.
2. For a detailed description of the LED interface and register information, refer to the IXF1110 Datasheet.

8.0 Test Points

8.1 Reset Test Points

Two test points allow evaluation of the IXF1110 reset signals. TP21 allows IXF1110 $\overline{\text{Sys\_Res}}$ signal monitoring. DTP3 allows board reset signal monitoring. The board $\overline{\text{Sys\_Res}}$ can be monitored on both test points if it is asserted by Switch S1 or the CPU. The reset is seen at TP21 if an IXF1110 reset is issued by the software interface.

Table 5. Intel® IXF1110 Reset Test Points

Test Point	Symbol	IXF1110 Ball Designator	Description
TP21	$\overline{\text{Sys\_Res}}$	Y4	System reset for IXF1110
DTP3	$\overline{\text{Sys\_Res}}$	–	Board reset
NOTE: DTP = Differential Test Point, TP = Test Point			

8.2 IXF1110 Input Clock Test Points

The IXF1110 requires input clocks of 50 and 125 MHz. There are two test points that allow the user to monitor those signals (see Table 6).

Table 6. Intel® IXF1110 Differential Input Clock Test Points

Test Point	Symbol	IXF1110 Ball Designator	Description
DTP1	CLK125	AA5	125 MHz input clock for IXF1110
DTP2	CLK50	C21	50 MHz input clock for IXF1110
NOTE: DTP = Differential Test Point			

8.3 GBIC Test Points

Table 7 lists GBIC test points that allow evaluation of the I^2C clock, which is connected to all of the GBIC modules, and the I^2C Data pins for each of the ten ports. For more information on the I^2C interface, refer to the IXF1110 Datasheet.

Table 7. GBIC Test Points (Sheet 1 of 2)

Test Point	Symbol	IXF1110 Ball Designator	Description
DTP6	I^2C_CLK	L19	I^2C_CLK for IXF1110
DTP7	I^2C_DATA_0	G22	I^2C_DATA_0 for IXF1110
DTP8	I^2C_DATA_1	G23	I^2C_DATA_1 for IXF1110
DTP9	I^2C_DATA_2	J24	I^2C_DATA_2 for IXF1110
DTP10	I^2C_DATA_3	F22	I^2C_DATA_3 for IXF1110
NOTE: DTP = Differential Test Point			

Table 7. GBIC Test Points (Sheet 2 of 2)

Test Point	Symbol	IXF1110 Ball Designator	Description
DTP11	I^2C_DATA_4	E23	I^2C_DATA_4 for IXF1110
DTP12	I^2C_DATA_5	H24	I^2C_DATA_5 for IXF1110
DTP13	I^2C_DATA_6	G20	I^2C_DATA_6 for IXF1110
DTP14	I^2C_DATA_7	E22	I^2C_DATA_7 for IXF1110
DTP15	I^2C_DATA_8	G24	I^2C_DATA_8 for IXF1110
DTP16	I^2C_DATA_9	F24	I^2C_DATA_9 for IXF1110
NOTE: DTP = Differential Test Point			

8.4 Mictor Connectors

Table 8 provides a detailed list of the Mictor Connector test points that are available using Mictor Connectors and that are designed for easy use with the Tektronix* P6434 Mass Termination Probe. Using these connectors with a Tektronix* logic analyzer allows the probing of the signals in Table 8.

Table 8. Mictor Connector Test Points (Sheet 1 of 2)

Probe A	CPU Data Bus	IXF1110 Ball Designator	Probe C	Address Bus and Other	IXF1110 Ball Designator	Probe D	Pause I/F and Reset Signals	IXF1110 Ball Designator
A0(0)	uPx_Data0	B3	C0(0)	TA	–	D0(0)	–	
A0(1)	uPx_Data1	A4	C0(1)	Start_XFER	–	D0(1)	–	
A0(2)	uPx_Data2	B9	C0(2)	RD/~WR	–	D0(2)	–	
A0(3)	uPx_Data3	A7	C0(3)	Gen_PCsN	–	D0(3)	–	
A0(4)	uPx_Data4	C12	C0(4)	–		D0(4)	–	
A0(5)	uPx_Data5	E11	C0(5)	CsN	–	D0(5)	–	
A06)	uPx_Data6	C13	C0(6)	Bus_request	–	D0(6)	–	
A0(7)	uPx_Data7	A8	C0(7)	Bus_Busy	–	D0(7)	–	
A1(0)	uPx_Data8	A10	C1(0)	Bus_Grant	–	D1(0)	–	
A1(1)	uPx_Data9	A9	C1(1)	–		D1(1)	–	
A1(2)	uPx_Data10	E12	C1(2)	uPx_RdyN	C22	D1(2)	–	
A1(3)	uPx_Data11	A11	C1(3)	–		D1(3)	–	
A1(4)	uPx_Data12	G12	C1(4)	uPx_CsN	F20	D1(4)	–	
A1(5)	uPx_Data13	E10	C1(5)	uPx_WrN	A18	D1(5)	–	
A1(6)	uPx_Data14	F11	C1(6)	uPx_RdN	H14	D1(6)	POR	–
A1(7)	uPx_Data15	D7	C1(7)	–		D1(7)	HRESET	–
A2(0)	uPx_Data16	D14	C2(0)	uPx_Add0	J1	D2(0)	–	
A2(1)	uPx_Data17	C14	C2(1)	uPx_Add1	G4	D2(1)	–	
A2(2)	uPx_Data18	F14	C2(2)	uPx_Add2	F3	D2(2)	–	
1. For evaluation of the signals provided by the Mictor connector, use the corresponding logic analyzer probe.								

Table 8. Mictor Connector Test Points (Sheet 2 of 2)

Probe A	CPU Data Bus	IXF1110 Ball Designator	Probe C	Address Bus and Other	IXF1110 Ball Designator	Probe D	Pause I/F and Reset Signals	IXF1110 Ball Designator
A2(3)	uPx_Data19	A12	C2(3)	uPx_Add3	H1	D2(3)	–	
A2(4)	uPx_Data20	A15	C2(4)	uPx_Add4	E3	D2(4)	–	
A2(5)	uPx_Data21	G13	C2(5)	uPx_Add5	E2	D2(5)	–	
A2(6)	uPx_Data22	B16	C2(6)	uPx_Add6	G1	D2(6)	–	
A2(7)	uPx_Data23	E15	C2(7)	uPx_Add7	C3	D2(7)	–	
A3(0)	uPx_Data24	G14	C3(0)	uPx_Add8	F5	D3(0)	–	
A3(1)	uPx_Data25	A16	C3(1)	uPx_Add9	F1	D3(1)	–	
A3(2)	uPx_Data26	C17	C3(2)	uPx_Add10	C2	D3(2)	–	
A3(3)	uPx_Data27	A17	C3(3)	–		D3(3)	TxPause Add3	K1
A3(4)	uPx_Data28	B18	C3(4)	–		D3(4)	TxPause Add2	J2
A3(5)	uPx_Data29	A21	C3(5)	–		D3(5)	TxPause Add1	G2
A3(6)	uPx_Data30	B22	C3(6)	–		D3(6)	TxPause Add0	G3
A3(7)	uPx_Data31	C23	C3(7)	IRQ	–	D3(7)	TxPause Fr	J7
CLK_0	Bus_CLK	–	CLK_3	–		Q0	–	–
CLK_1	–		Q1	–		CLK_2	–	–

1. For evaluation of the signals provided by the Mictor connector, use the corresponding logic analyzer probe.

8.5 Power and Ground Test Points

Table 9 provides the power and ground test points that allow the monitoring of voltages at various points on the board.

Table 9. Power Test Points (Sheet 1 of 2)

Test Point	Symbol	Description
TP2	Vdd_1P8_IXF	1.8 V for IXF1110
TP3	Vdd_2P5_IXF	2.5 V for IXF1110
TP4	TxA25_A	SerDes Tx Block A 2.5 V
TP5	PLL1_aVdd	1.8 V for PLL1
TP6	PLL2_aVdd	1.8 V for PLL2
TP8	PLL3_aVdd	2.5V for PLL3
TP9	TxA25_C	SerDes Tx Block C 2.5 V
TP19	Vdd_2P5	2.5 V rest of the board

NOTE: TP = Test Point

Table 9. Power Test Points (Sheet 2 of 2)

Test Point	Symbol	Description
TP20	Vdd_3P3	3.3 V rest of the board
TP22	TxAVTT_A	SerDes Tx Block A 1.8 V
TP23	TxAVTT_B	SerDes Tx Block B 1.8 V
TP24	RxAVTT_C	SerDes Rx Block C 1.8 V
TP25	RxA25_A	SerDes Rx Block A 2.5 V
TP26	RxAVTT_A	SerDes Rx Block A 1.8 V
TP27	TxA25_B	SerDes Tx Block B 2.5 V
TP28	RxA25_B	SerDes Rx Block B 2.5 V
TP29	RxAVTT_B	SerDes Rx Block B 1.8 V
TP30	TxAVTT_C	SerDes Tx Block C 1.8 V
TP31	RxA25_C	SerDes Rx Block C 2.5 V
NOTE: TP = Test Point		

Table 10 lists the various ground test points provided on the IXD1110 demo board.

Table 10. Ground Test Points

Test Point	Symbol	Description
TP10	GND	Ground Test Points
TP11		
TP12		
TP13		
TP14		
TP15		
TP16		
TP17		
NOTE: TP = Test Point		

8.6 Unused Test Points

The unused test points are for internal testing only and are not designed for evaluation of the IXF1110 device. Table 11 provides a list of the unused test points.

Table 11. Unused Test Points

Test Points	Description
J29	J29, J30, 31, J32, J33, J34, and TP1 are not designated for IXF1110 evaluation
J30	
J31	
J32	
J33	
J34	
TP1	

9.0 Board Schematics

Figure 4. Intel® IXD1110 Demo Board Power (Revision A1)

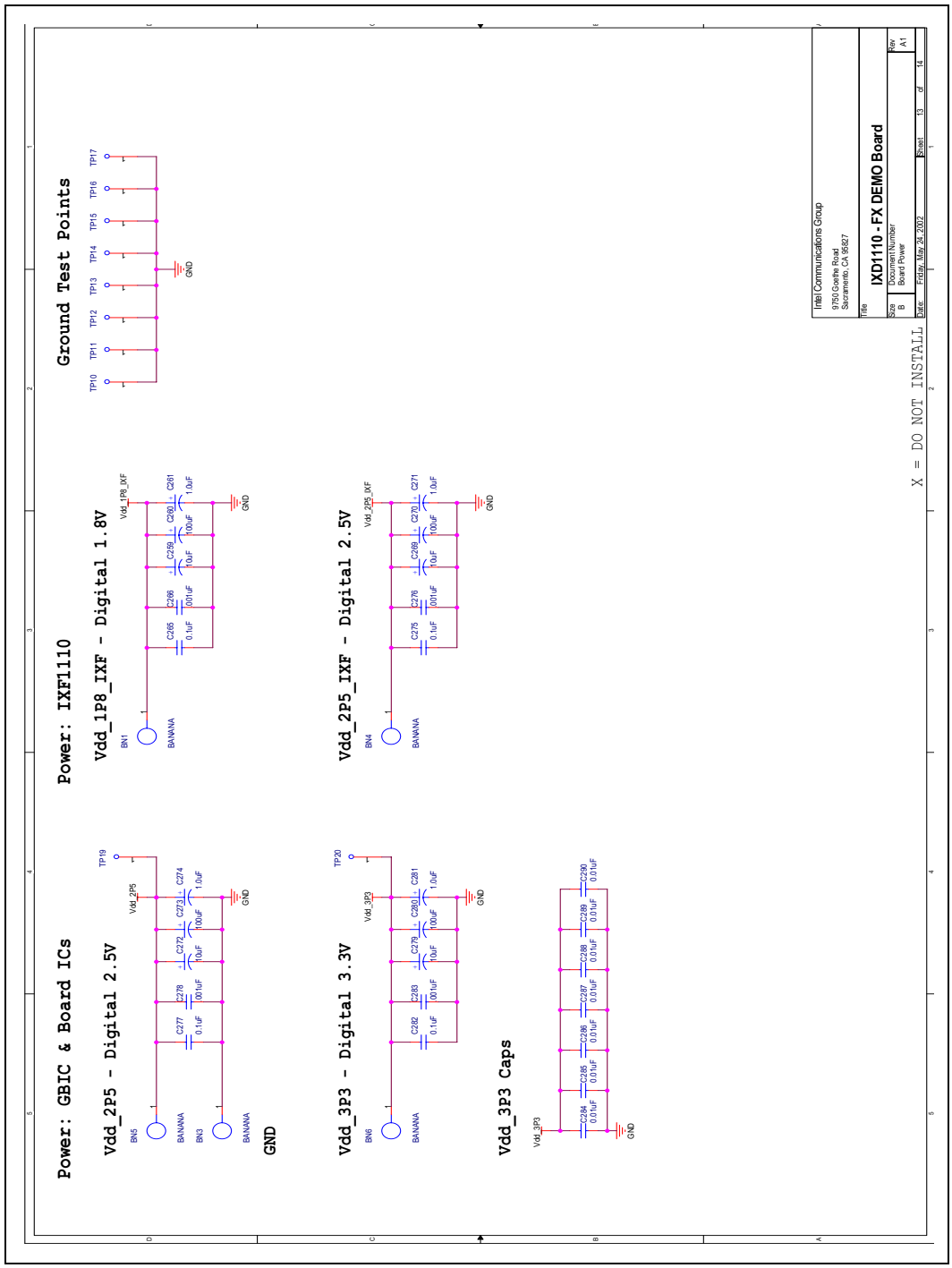


Figure 5. Intel® IXD1110 Digital Power

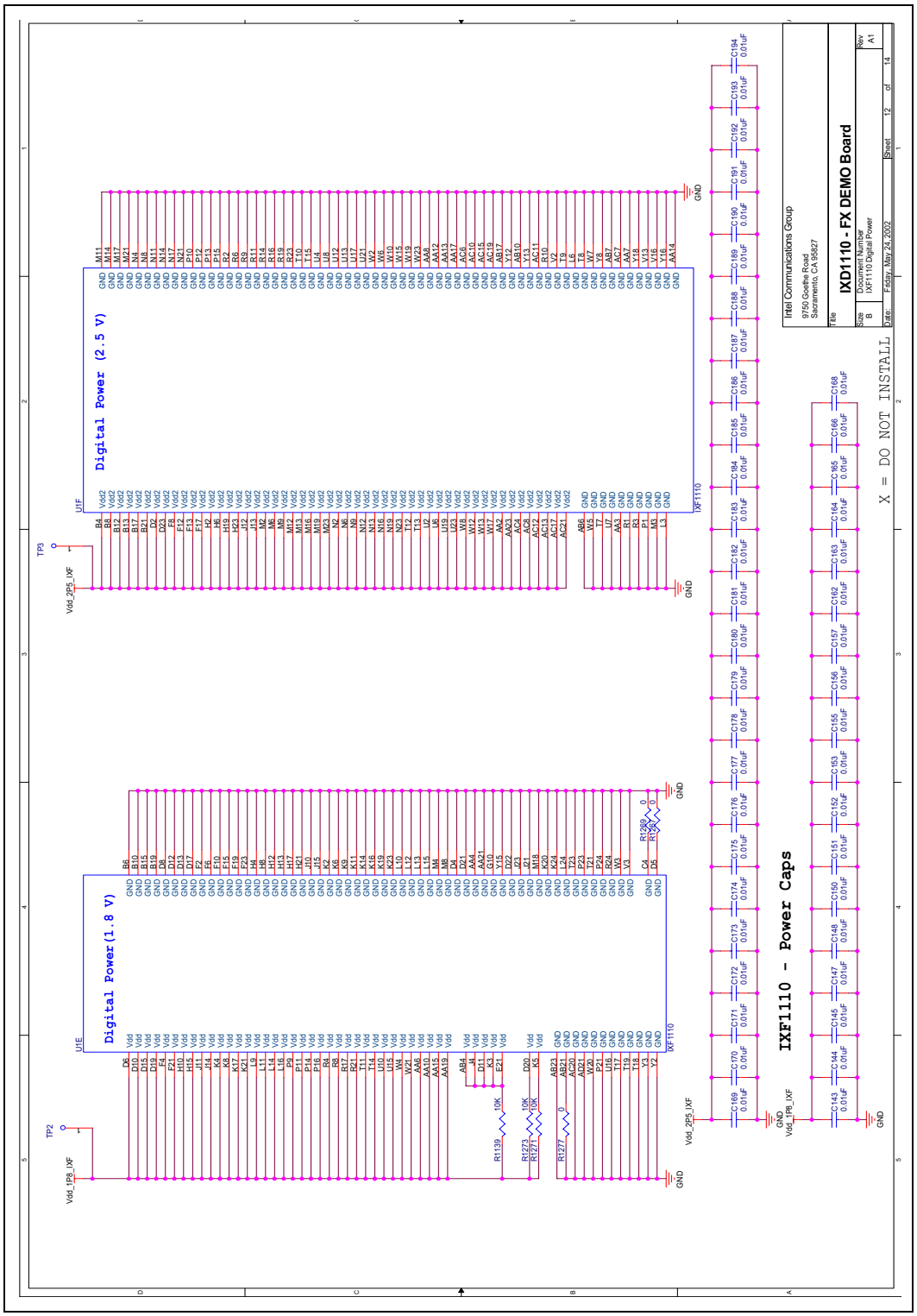


Figure 6. Intel® IXD1110 Analog Power

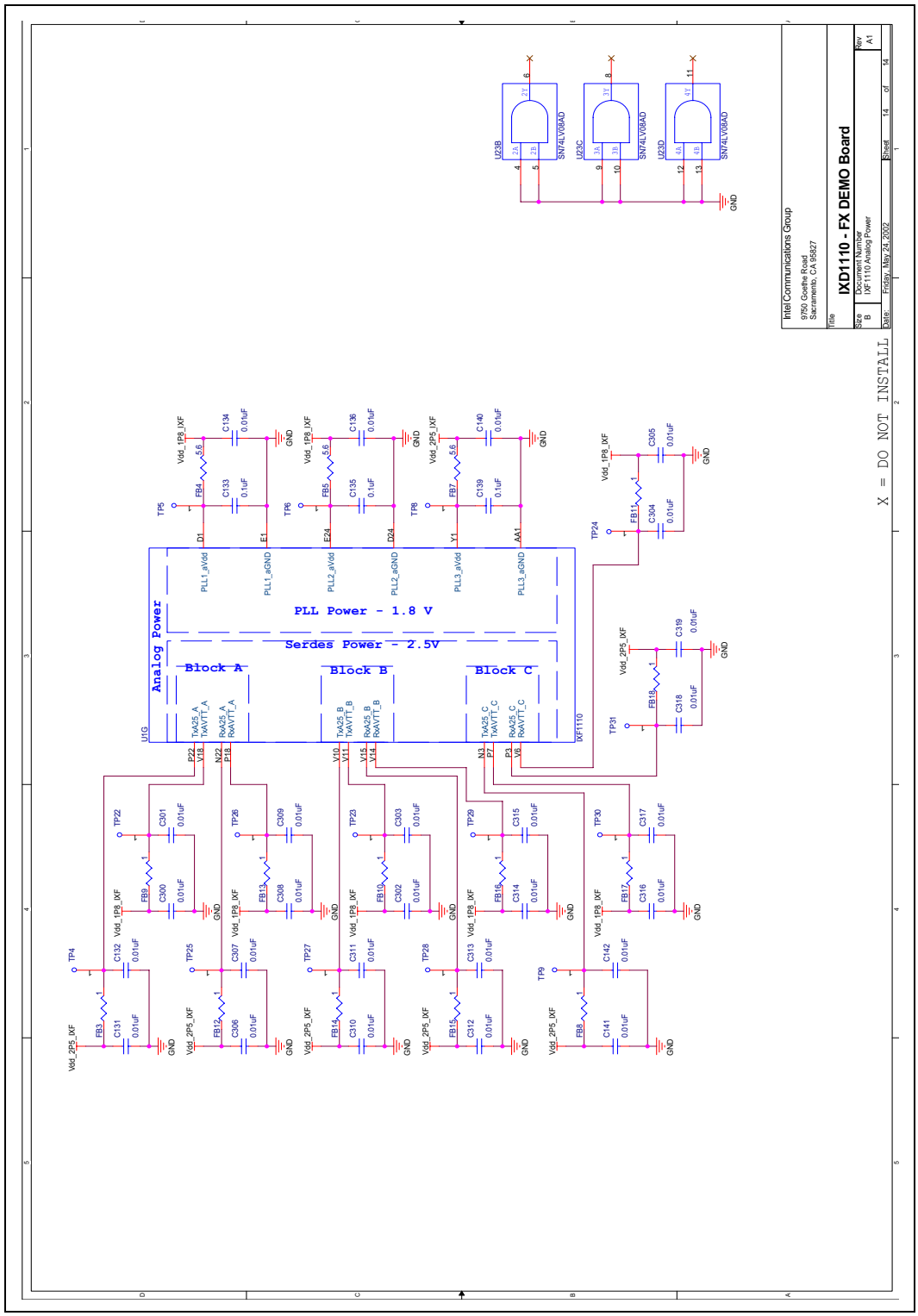


Figure 7. Intel® IXD1110 Control

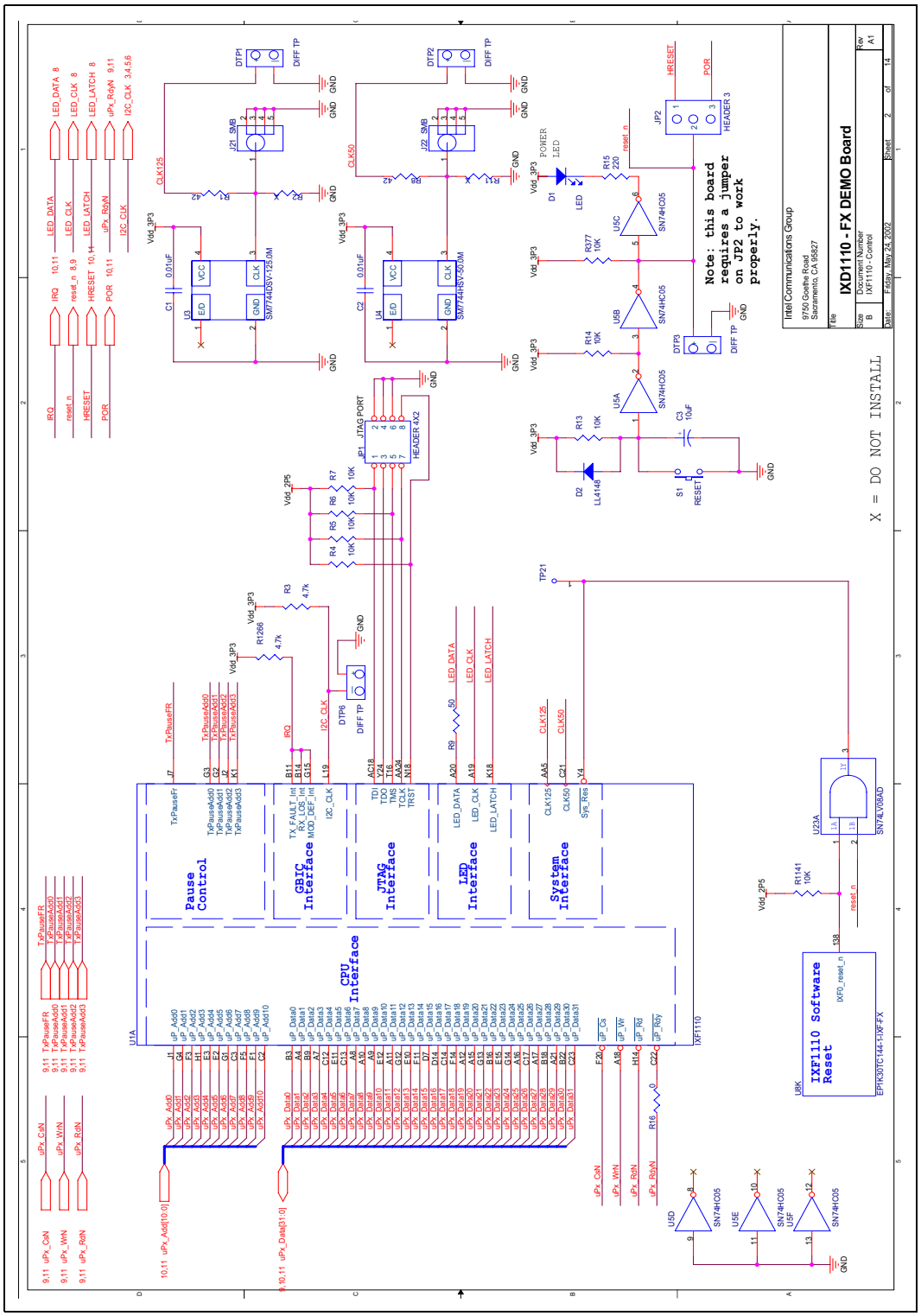


Figure 8. Intel® IXD1110 SerDes GBIC Ports 0-2

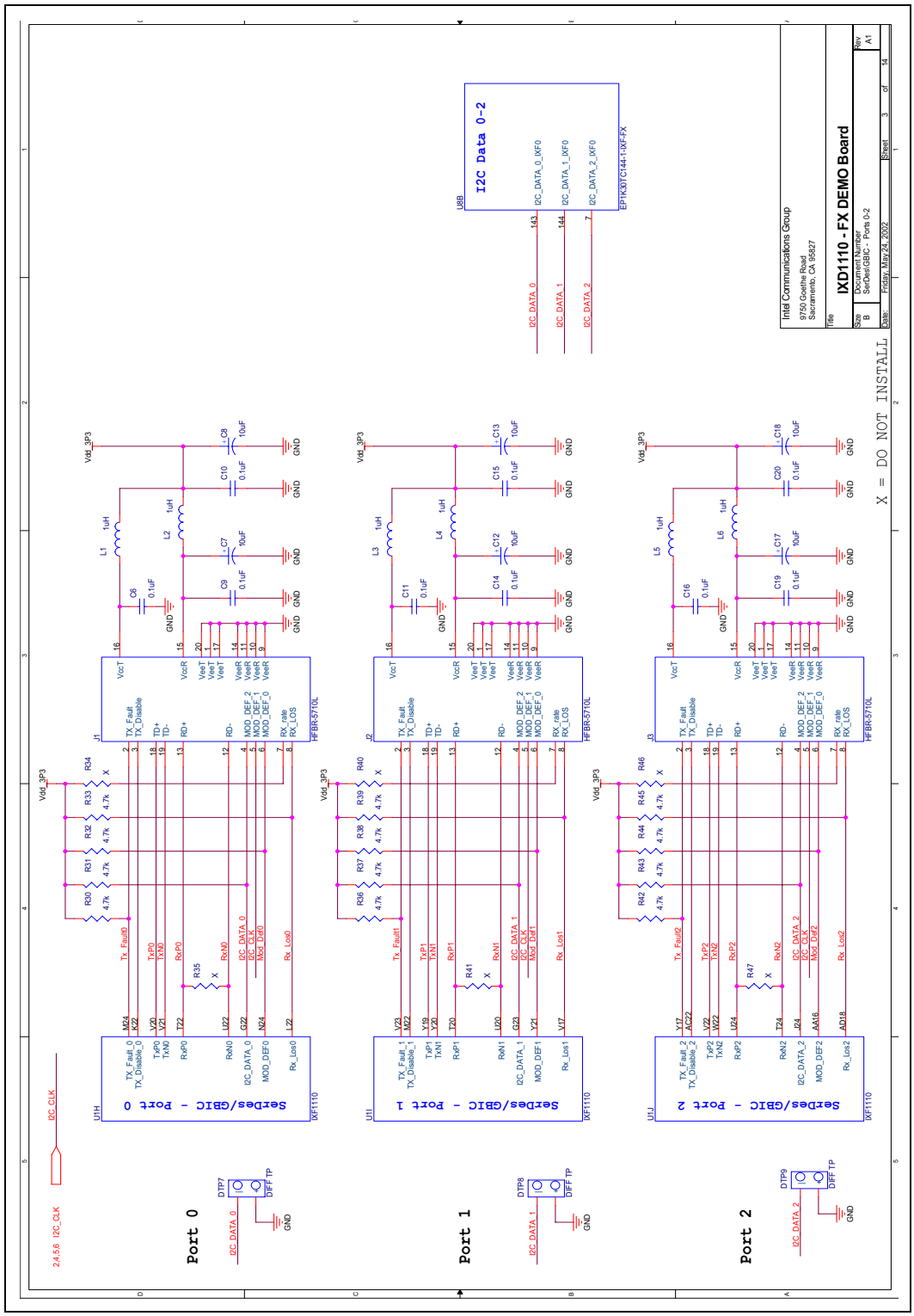


Figure 9. Intel® IXD1110 SerDes GBIC Ports 3-5

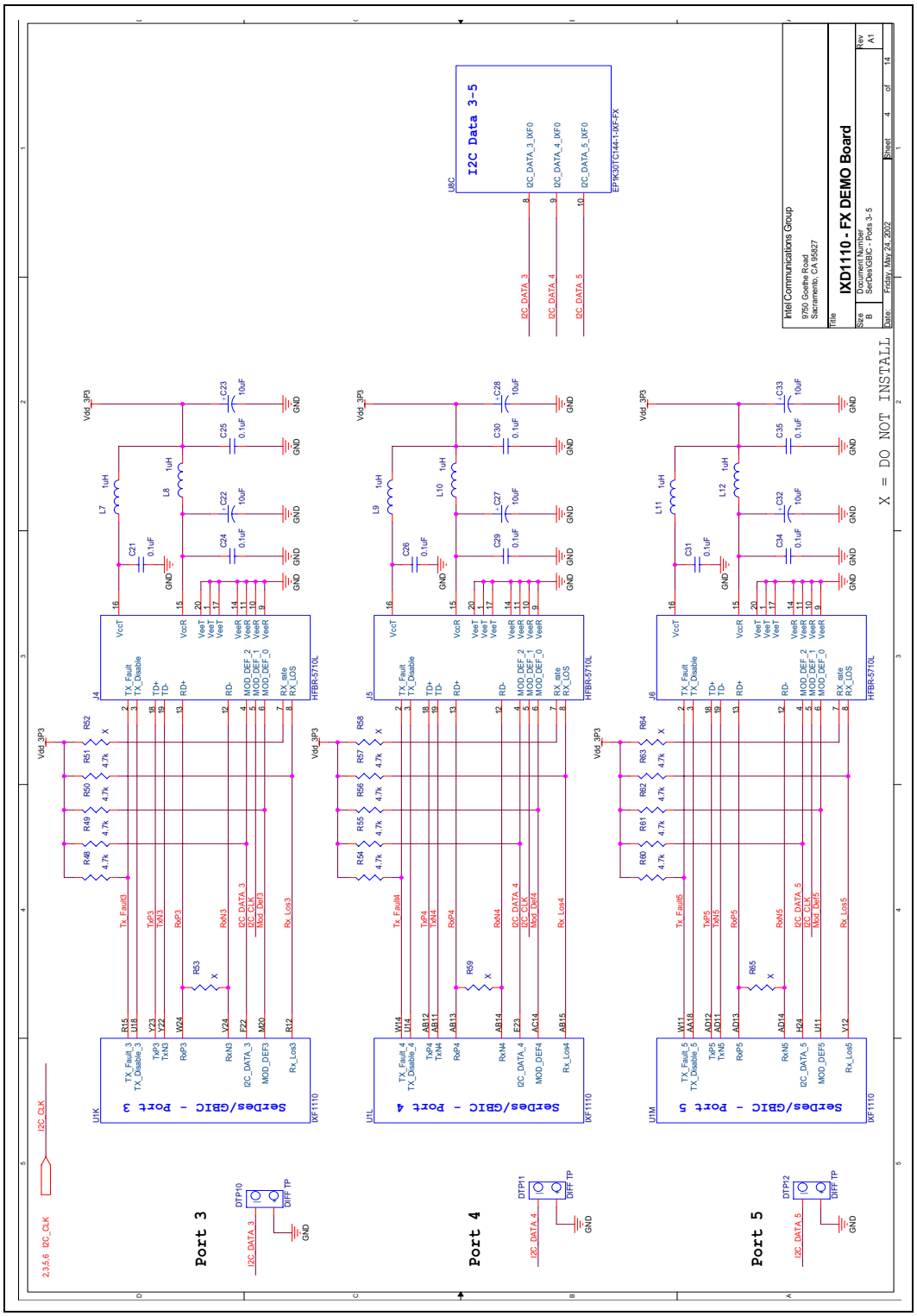


Figure 10. Intel® IXD1110 SerDes GBIC Ports 6-8

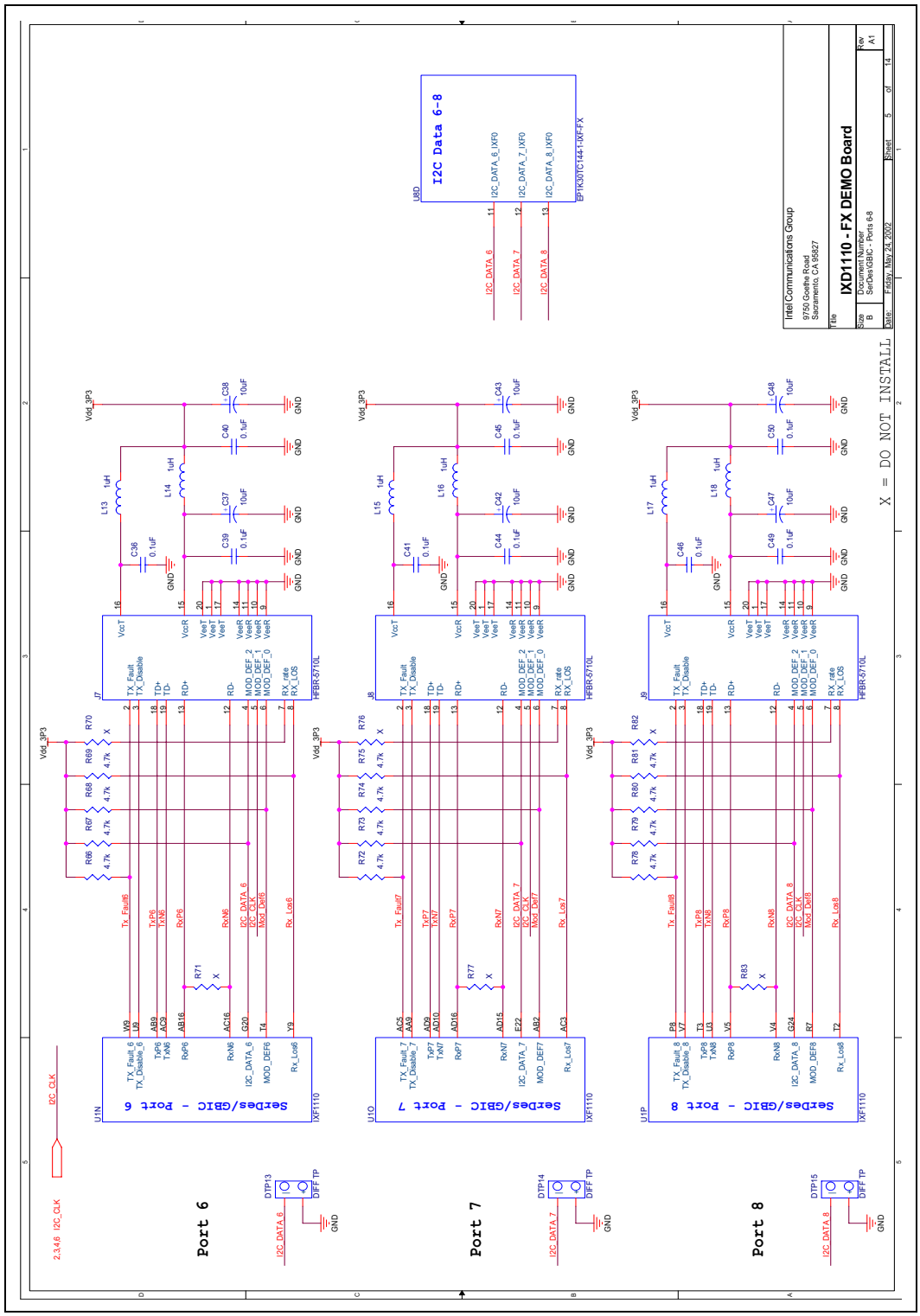


Figure 11. Intel® IXD1110 SerDes GBIC Port 9

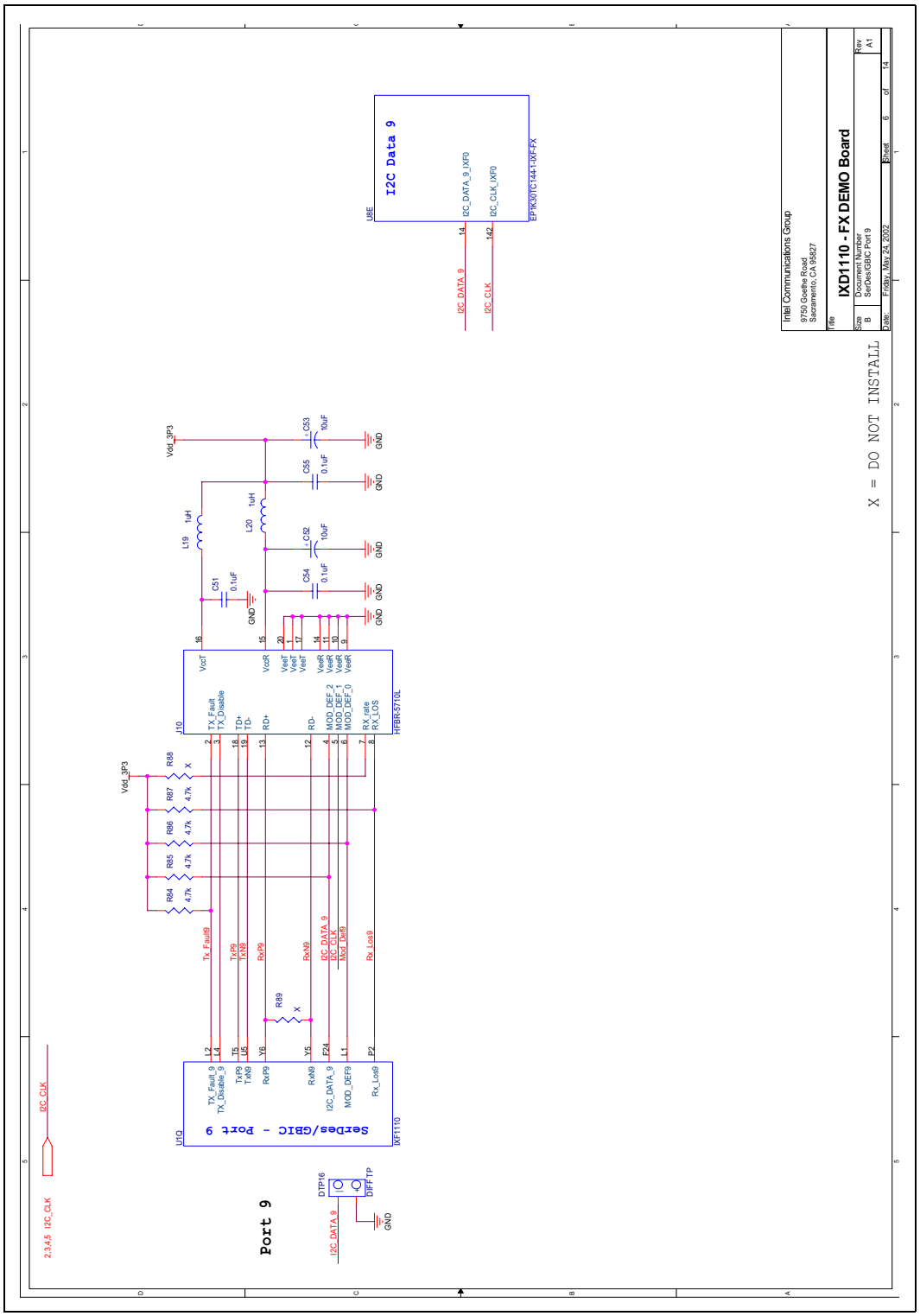


Figure 12. Intel® IXD1110 SPI4-2

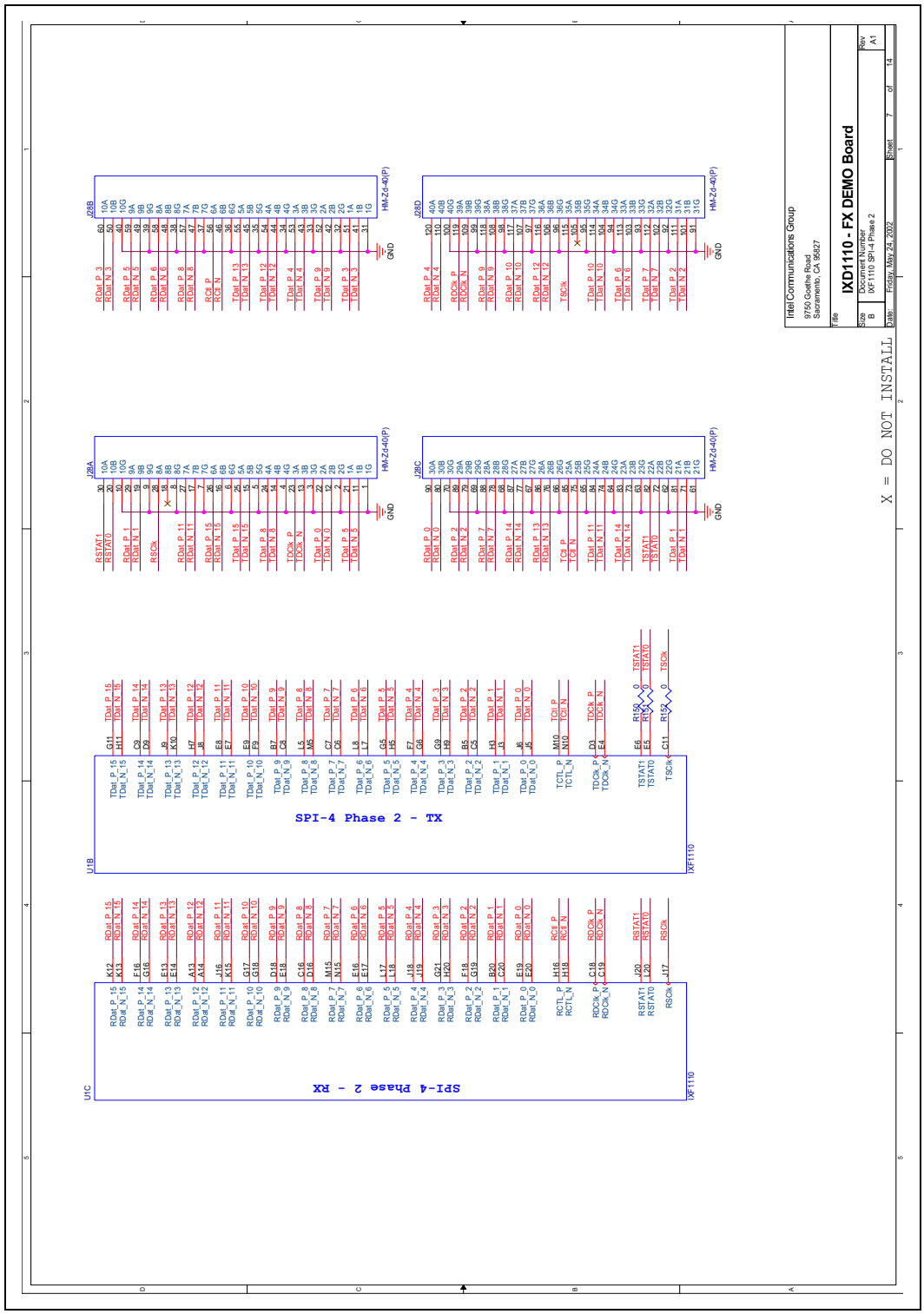


Figure 13. Intel® IXD1110 LEDs

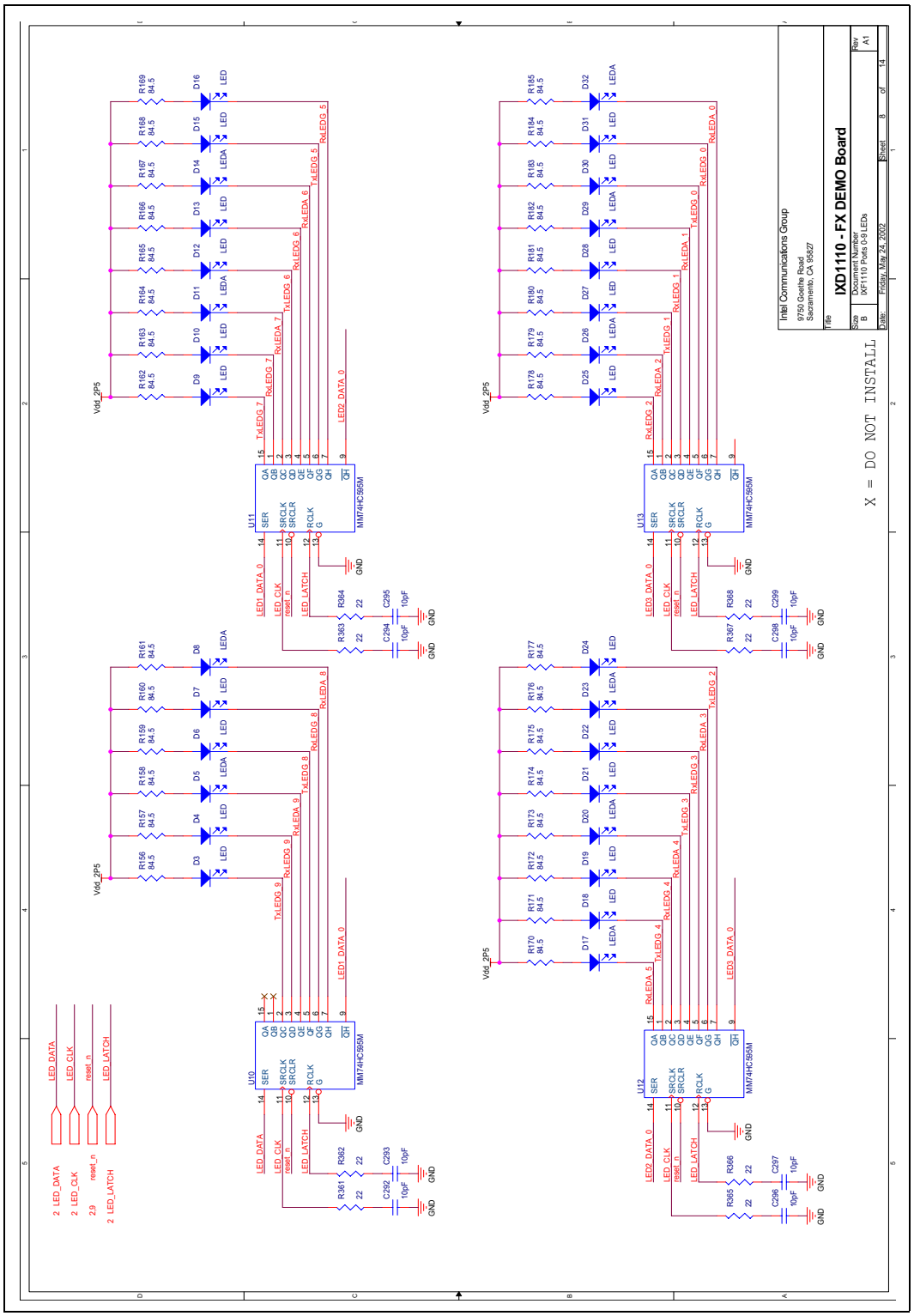


Figure 14. Intel® IXD1110 CPU Interface Control

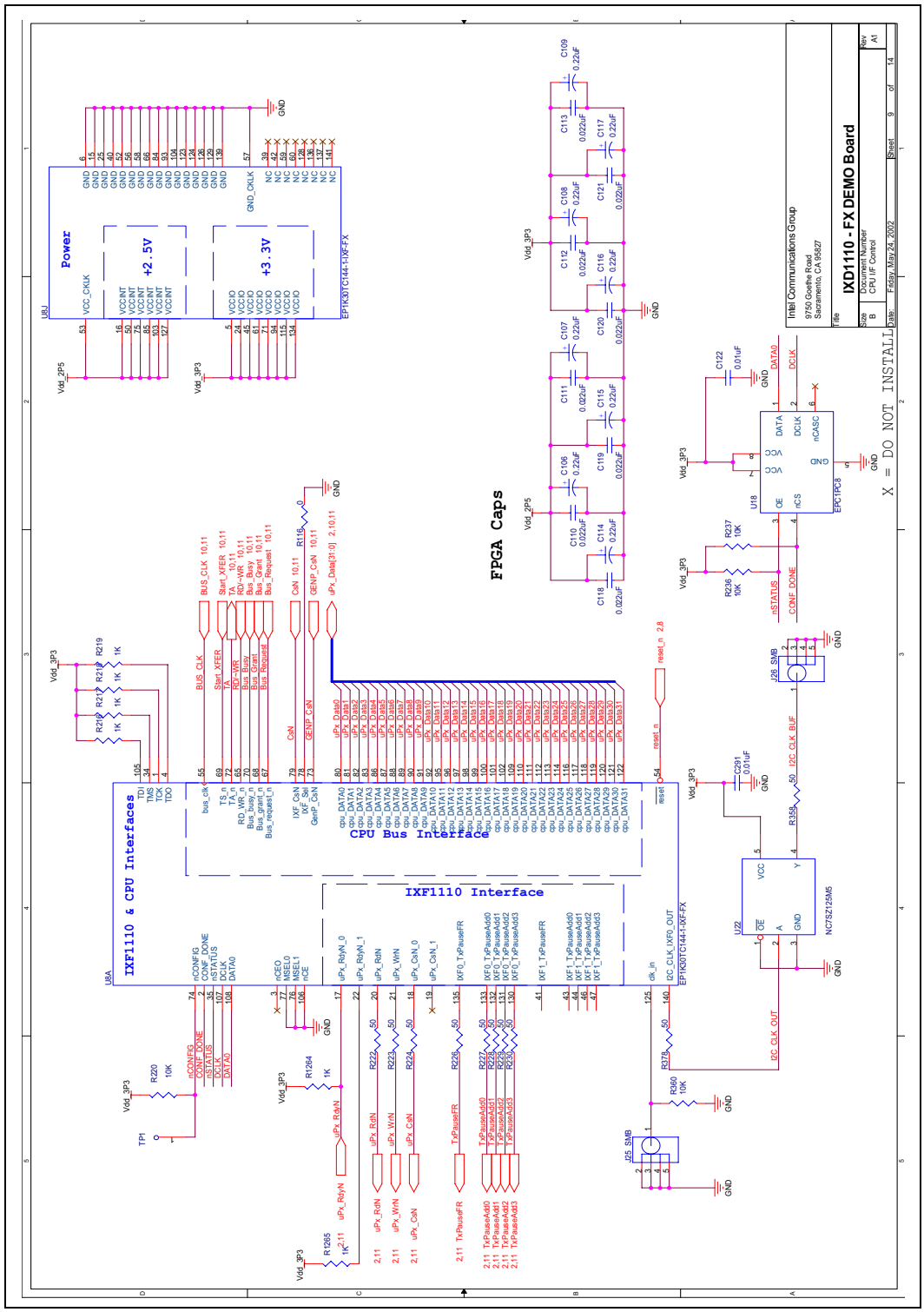


Figure 15. Intel® IXD1110 CPU Connectors

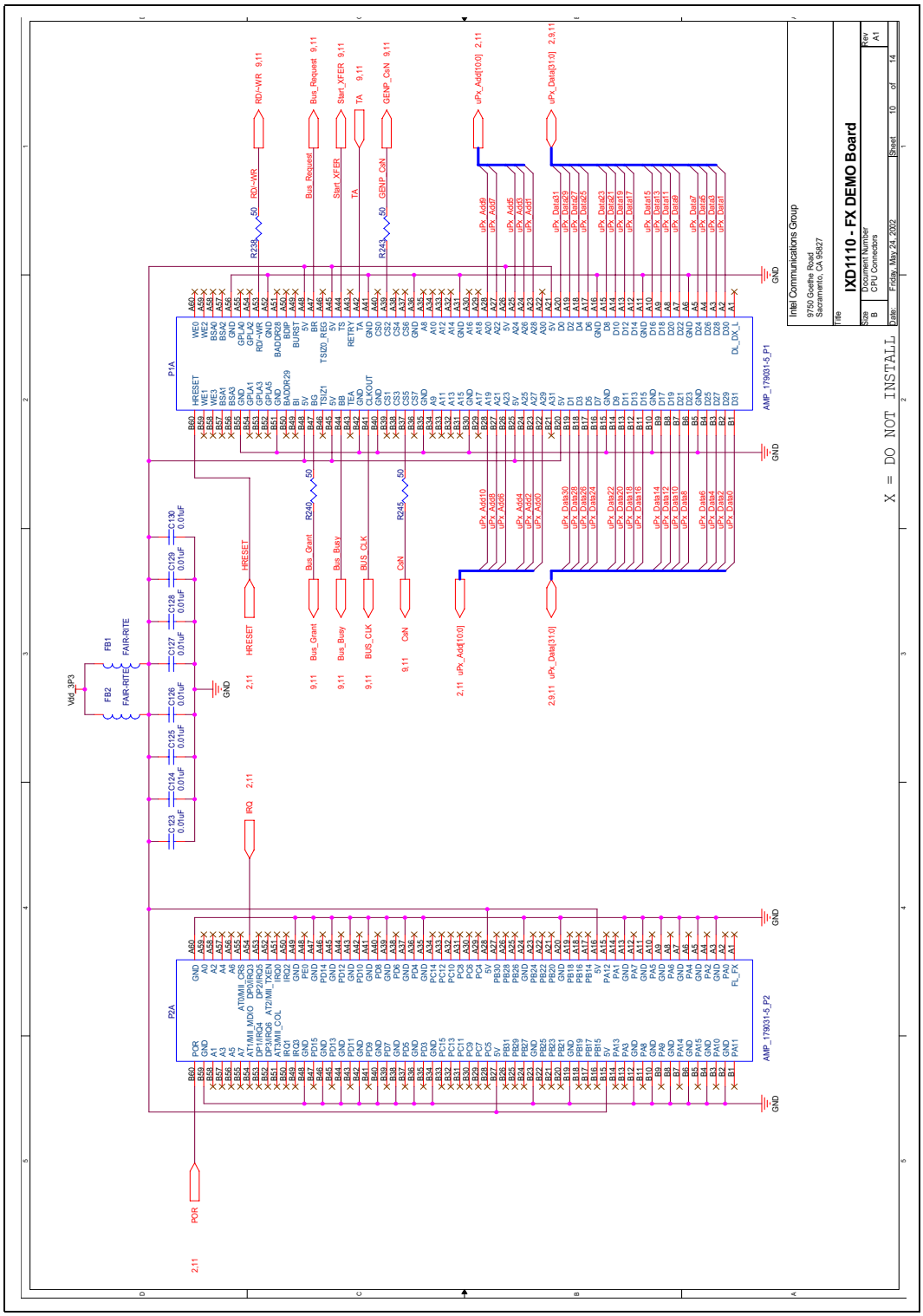
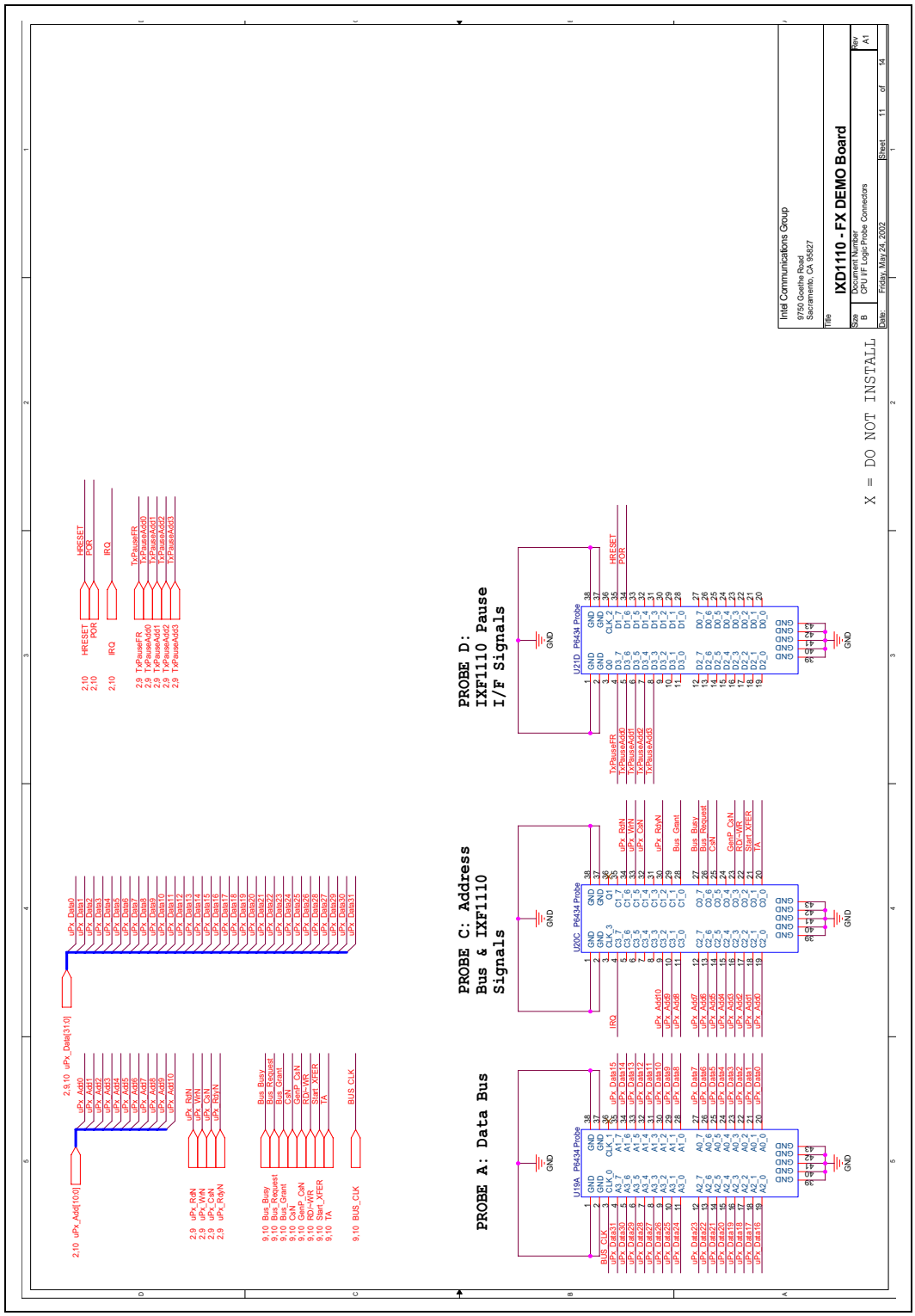


Figure 16. Intel® IXD1110 CPU Logic Probe Connectors


PROBE A: Data Bus
PROBE C: Address Bus & IXF1110 Signals
PROBE D: IXF1110 Pause I/F Signals
X = DO NOT INSTALL
Intel Communications Group
9750 Goethe Road
Sacramento, CA 95827
IXD1110 - FX DEMO Board
CPU I/F Logic Probe Connectors
Friday, May 24, 2002

10.0 Bill of Materials

Table 12. Intel® IXD1110 Demo Board Bill of Materials (Rev. A1)

Reference Designator	Description	Manufacturer[1]	Part Number
BN1, 3-6	CONN BANANA NUT SILVER	EF Johnson	108-0740-001
C1-2, 122-132, 134, 136-138, 140-145, 147-148, 150-153, 155-157, 162-166, 168-194, 300-319	CAP .01UF 16V CER 10% X7R (0603)	Panasonic	ECJ-1VB1C103K
C3, 7-8, 12-13, 17-18, 22-23, 27-28, 32-33, 37-38, 42-43, 47-48, 52-53	CAP 10UF 16V TANT SIZE B (CASEB)	Vishay	293D106X9016B
C6, 9-11, 14-16, 19-21, 24-26, 29-31, 34-36, 39-41, 44-46, 49-51, 54-55, 133, 135, 139, 265, 275, 277, 282	CAP 0.1UF 16V X7R (0603)	Panasonic	ECJ-1VB1C104K
C106-109, 114-117	CAP 0.22UF 35V TANT (CASEA)	Panasonic	ECS-H1VY224R
C110-113, 118-121	CAP .022UF 25V 10% CER (0603) SMD	Panasonic	ECU-V1E223KBV
C259, 269, 272, 279	CAP 10UF 16V TANT (CASEC)	Kemet	T491C106K016AS
C260, 270, 273, 280	CAP 100UF 25V ELEC FC RADIAL	Panasonic	EEU-FC1E101S
C261, 271, 274, 281	CAP 1.0UF 25V TANT (CASEA)	Panasonic	ECS-T1EY105R
C266, 276, 278, 283	CAP 1000PF 50V X7R (0603)	Panasonic	ECJ-1VB1H102K
C292-299	CAP 10PF +/- 0.5PF 50V NPO (0603) SMD	Panasonic	ECJ-1VC1H100D
D1, 3-4, 6-7, 9-10, 12-13, 15-16, 18-19, 21-22, 24-25, 27-28, 30-31	DIODE GREEN LED SS TYPE LOW CUR SMD	Panasonic	LNJ308G8LRA
D2	DIODE LL4148 SMD ( )	Diodes, Inc.	LL4148
D5, 8, 11, 14, 17, 20, 23, 26, 29, 32	DIODE AMBER LED SS TYPE LOW CUR SMD	Panasonic	LNJ408K8ZRA
DTP1-3, 6-16	HEADER 2X1	Berg	68000-240-2
FB1-2	FBEAD	Fair-Rite	2961666671
FB3, 8-18	RES 1.0 OHM 1/ 8W 1% (0805) SMD	Panasonic	ERJ-6RQF1R0V
FB4, 5, 7	RES 5.6 OHM 1/ 8W 1% (0805) SMD	Panasonic	ERJ-6RQF5R6V
J1-10	HOST CONN FOR HFBR-5701L	AMP	1367073-1

1. Third-party brands and names are the property of their respective owners.

Table 12. Intel® IXD1110 Demo Board Bill of Materials (Rev. A1) (Continued)

Reference Designator	Description	Manufacturer[1]	Part Number
J1-10	MISC BOTTOM EMI CAGE FOR HFBR-5710L	AMP	1367034-1
J1-10	MISC TOP EMI CAGE FOR HFBR-5710L	AMP	1367035-1
J1-10	IC FIBER MODULE HFBR-5710	Agilent	HFBR-5710L
J25-26	CONN SMB STRAIGHT JACK RECPT	Johnson Components	131-3711-201
J28	HEADER 40 DIFF PAIR 120 PIN	AMP	1469002-1
JP1	HEADER 4X2	Berg	C9192-280-4
JP2	HEADER 3X1	Berg	68000-240-3
L1-20	INDUCTOR 1UH SMD (1206)	TDK	MLF3216A1R0KT000
P1-2	CONN PLUG ASSY 120 POS .8MM FHBB	AMP	179031-5
R1, 8	RES 42.2 OHM 1/16W 1% (0603)	Panasonic	ERJ-3EKF42R2V
R2, 11, 34-35, 40-41, 46-47, 52-53, 58-59, 64-65, 70-71, 76-77, 82-83, 88-89	NOT INSTALLED		
R3, 30-33, 36-39, 42-45, 48-51, 54-57, 60-63, 66-69, 72-75, 78-81, 84-87, 1266	RES 4.75K 1/16W 1% (0603)	Panasonic	ERJ-3EKF4751V
R4-7, 13-14, 220, 236-237, 360, 377, 379-389, 1139, 1141, 1271, 1273	RES 10K 1/16W 1% (0603)	Panasonic	ERJ-3EKF1002V
R9, 116, 222-224, 226-230, 238, 240, 243, 245, 358, 378, 390	RES 49.9 OHM 1/16W 1% (0603)	Panasonic	ERJ-3EKF49R9V
R15	RES 221 OHM 1/16W 1% (0603)	Panasonic	ERJ-3EKF2210V
R16, 150-152, 1267, 1269, 1277	RES 0 OHM 1/16W 5% (0603) SMD	Panasonic	ERJ-3GEY0R00V
R156-185	RES 84.5 OHM 1/16W 1% (0603) SMD	Panasonic	ERJ-3EKF84R5V
R216-219, 1264, 1265	RES 1.00K 1/16W 1% (0603)	Panasonic	ERJ-3EKF1001V
R361-368	RES 22.1 OHM 1/16W 1% (0603)	Panasonic	ERJ-3EKF22R1V
S1	SWITCH SPST MOM KEY J-LEAD SMD	C&K Components	KT11P2JM
TP1	HEADER 1X1	Berg	68000-240-1

1. Third-party brands and names are the property of their respective owners.

Table 12. Intel® IXD1110 Demo Board Bill of Materials (Rev. A1) (Continued)

Reference Designator	Description	Manufacturer[1]	Part Number
TP2-17, 19-21	TESTPOINT SILVER LOOP (SMD)	Components Corp. (Lab stock-reel)	TP-108-02
U1	IC MAC IXF1110 10 PORT	Intel	IXF1110
U3	OSC 125 MHZ 3.3V 4 PIN SMD	Pletronics	SM7744DSV-125.0M
U4	OSC 50.0 MHZ 3.3V 4 PIN SMD	Pletronics	SM7744HSV-50.0M
U5	IC LOGIC 74HC05 HEX INVERTER W/ OD 14 PIN SOP	Texas Instruments	SN74HC05D
U8	IC FPGA EP1K30TC144-1	Altera	EP1K30TC144-1
U10-13	IC LOGIC 74HC595 8 BIT SHIFT REGISTER 16 PIN SOIC	Fairchild Semiconductor	MM74HC595M
SOCKET FOR U18	SOCKET 8 PIN DIP GOLD	MILL--Max Manufacturing Corp	110-93-308-41-001
U18	IC MEM PROM EPC1PC8 ALTERA 8 PIN DIP (DIP8)	Altera	EPC1PC8
U19-21	CONN 38 PIN MICTOR PLUG CONNECTOR ( )	AMP	2-767004-2
LATCH HOUSING FOR U19-21	MISC LATCH HOUSING FOR MICTOR RECPT	Precision Interconnect	105-1089-00
U22	IC LOGIC NC7SZ125 SINGLE TRISTATE BUFFER SOT23	Fairchild Semiconductor	NC7SZ125M5
U23	IC LOGIC 74LV08 QUAD 2-INPUT AND GATE 14 SOP	Texas Instruments	SN74LV08AD

1. Third-party brands and names are the property of their respective owners.